IN THE CLAIMS:

Please consider the claims as follows:

1. (Currently Amended) A method for evaluating reliability of a semiconductor chip structure built by a manufacturing process, comprising the steps of:

building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure;

thermal cycling the test structure;

measuring ~~the~~ a yield of the test structure; and

evaluating reliability of the semiconductor chip structure built by the manufacturing process based on the yield of the test structure.

2. (Original) The method as recited in claim 1, wherein the yield includes a relative number of electrically functional structures formed by the manufacturing process before thermal cycling.

3. (Original) The method as recited in claim 1, further comprising the step of fabricating the test structure to provide a uniform stress condition on one or more structures.

4. (Original) The method as recited in claim 1, wherein the step of building includes employing a dual damascene process.

5. (Original) The method as recited in claim 4, wherein the step of building includes forming the dual damascene structure with vias having conductive liners along bottoms and sidewalls of the vias.

6. (Original) The method as recited in claim 1, wherein the step of building a test structure includes providing a mismatch in a coefficient of thermal expansion (CTE) between metal and dielectric materials.

7. (Original) The method as recited in claim 1, wherein the step of building includes building the test structure to provide a bimodal failure distribution having early and late fails during thermal cycle testing.

8. (Original) The method as recited in claim 7, wherein the step of evaluating reliability is based on early fails.

9. (Currently Amended) A method for evaluating reliability of a semiconductor chip structure built by a manufacturing process, comprising the steps of:

building a test structure in accordance with a manufacturing process used in fabricating a semiconductor chip structure to test reliability of the semiconductor chip structure, the test structure using, ~~which uses~~ materials having mismatches in coefficients of thermal expansion, the test structure including features having predetermined strain values;

thermal cycling the test structure to induce changes or failures of the features;

measuring ~~the~~ a yield of the features in the test structure; and

evaluating reliability of the semiconductor chip structure built by the manufacturing process based on the yield of the test structure.

10. (Original) The method as recited in claim 9, wherein the yield includes a relative number of electrically functional features formed by the manufacturing process before thermal cycling.

11. (Original) The method as recited in claim 9, further comprising the step of fabricating the test structure to provide a uniform stress condition on one or more of the features.

12. (Original) The method as recited in claim 9, wherein the step of building includes employing a dual damascene process to form the features.

13. (Original) The method as recited in claim 12, wherein the step of building includes forming dual damascene features with vias having conductive liners along bottoms and sidewalls of the vias.

14. (Original) The method as recited in claim 9, wherein the step of building a test structure includes providing a mismatch in a coefficient of thermal expansion (CTE) between metal and dielectric materials.

15. (Original) The method as recited in claim 9, wherein the step of building includes building the test structure to provide a bimodal failure distribution having early and late fails.

16. (Original) The method as recited in claim 15, wherein the step of evaluating reliability is based on early fails.

17-31. (Canceled)

32. (New) The method as recited in claim 1, wherein building a test structure includes building a via chain through layers of the semiconductor chip structure such that a plurality of widths of the vias are used to adjust strain in different layers.

33. (New) The method as recited in claim 1, wherein building a test structure includes building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure.

34. (New) The method as recited in claim 9, wherein building a test structure includes building a via chain through layers of the semiconductor chip structure such that a plurality of widths of the vias are used to adjust strain in different layers.

35. (New) The method as recited in claim 9, wherein building a test structure includes

building a dummy structure to provide a via density in an area of the semiconductor chip structure to adjust strain in adjacent structures of the test structure.